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From:

Richard J. Coldren, Esq.

Date:

December 18, 2002

Client/Matter No.: 013721-074563

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*transmittal letter x2 APTO/SB/08A

Applicant(s) Keeth et al. Serial No. 08/801,628 *PTO/SB/08B (2pp) *copies of 33 references Serial No. _ 08 March 2001 Filing Date Amount of Check N/A Atty's File No. DB000575-010 ELP/CFO/mk

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The dating stamp of the USPTO on this card 07 June 2001 will be taken as an indication that the accompanying paper(s) was filed.

Applicant(s) Keeth et al. *transmittal letter x2 *PTO/SB/08A *PTO/SB/08B (2pp)
Filing Date 08 March 2001 *copies of 33 references
Amount of Check N/A Atty's File No. DB000575-010 ELP/CFO/mk

The dating stamp of the USPTO on this card will be taken as an indication that the accompanying paper(s) was filed.

Applicant(s) <u>Keeth</u>
Title 256 MEG Dynamic Access Memory
Pages of Spec. 233 No. of Claim 30
Sheets of Drawings 367
Verified Strot.

Sheets of Drawings 367

Declaration X Verified Stmt.

Amt. of Check 9710 and \$1088

Atty's File No. DB000575-010

DOCKETED

ELP:sh

08 March 2001

*PTG/SB/05
*PTO/SB/17 (x2)
*Preliminary Amendment
*Microfiche Appendix
*Statement re
Deletion of Inventors
*Change of Address

09/601628

MAR 2 6 2001



PTO/SB/05 (11-00)

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UTILITY			Attorney Docket No. DB000575-010			
PATENT APPLICATION		First	First Inventor Keeth			
TRANSMITTAL		Title	Title 256 MEG Dynamic Access Memory			
(Only for new nonprovision	nal applications under 37 CFR 1.53(b)) Expre	ss Mail Label No.	EJ11653	8197US	
	ATION ELEMENTS coming utility patent application cont		DRESS TO:	Assistant Com Box Patent Ap Washington, I		atents
1. X Fee Transmittal Form (e.g., PTO/SB/17) Submit on original and a deplicate for five pressuring Applicant claims small entity shatus. See 37 CFR 1.27. 3. X Specification (prehamed analysment ast total below) - Descriptive title of the invention - Cross Reference to Related Applications - Statement Regarding Fed spensored R & D - Reference to sequences listing, a table, or a computer program listing appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(e) - Abstract of the Disclosure: 4. X Drawing(s) (35 U.S.C. 113) [Total Sheets 367] 5. Oath or Declaration [Total Pages] Nawly executed (original or copy) Copy from a prior application (37 CFR 1.63 (d)) (for continuation/divisional with Box 18 complisted) I. X DELETION OF INVENTOR(S) Signed abstement attached defailing inventor(s) nemed in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).			7. CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. Computer Readable Form (CRF) b. Specification Sequence Listing on: i. CD-ROM or CD-R (2 copies); or ii. paper c. Statements verifying Identity of above copies ACCOMPANYING APPLICATION PARTS 9. Assignment Papers (cover sheet & document(s)) 10. 37 CFR 3.73(b) Statement Power of (when there is an assignee) Attorney 11. English Translation Document (if applicable) 12. Information Disclosure Copies of IDS Statement (IDS)/PTO-1449 13. X Preliminary Amendment 14. Return Receipt Postcard (MPEP 503) (Should be specifically Iterrized) 15. (critised Copy of Printing Document(s) (if foreign priority is dealined) 16. Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35			
	Sheet. See 37 CFR 1.76	17.	or its equivalen			
18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76: OS 916,692						
19. CORRESPONDENCE ADDRESS						
Customer Number or Bar Co			or L	Corresponde	Ince address below	
Name	Edward L. Pencoske		7-11			
	Thorp Reed & Armstrong, LLP					
Address	One Oxford Centre, 1 Pittsburgh	4th Fl.,	301 Grant St		15219	,
City	1 12 C S D G I G I	State	 	Zip Co		
Country	U.S.A.	Telephone	412/394-7789		1475234	2555
Name (Print/Type)	Edward L. Pencoske	Re ₁	gistration No. (Attor		29,688	
Signature	la entimated to take 0,2 hours to complete	Time will year	depending upon the nex		8 March 2	
a smount of time you are require	ed to complete this form should be sent in R COMPLETED FORMS TO THIS ADD	the Chief Info	mation Officer, U.S. Pat	motesT beating	ark Office, Wash	ington. Di

I hereby certify that this correspondence is being deposited in the United States Postal Services as First Class Mail in an envelope address to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

Attorney for Applicant

Date: 4 June 2001

PATENT Attorney Docket No. DB000575-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

256 MEG DYNAMIC RANDOM ACCESS MEMORY

TRANSMITTAL LETTER FOR RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS - FILING DATE GRANTED

Assistant Commissioner for Patents ATTN: Box MISSING PARTS Washington, D.C. 20231

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Dear Sir:

Entitled:

OFFICE OF PETITIONS

This is in response to the Notice to File Corrected Application Papers - Filing Date Granted OF PETITIONS

(hereinafter "the Notice") mailed on April 30, 2001 in the above-captioned application having a shortened two month statutory period of response.

Enclosed herewith are the following:

- 1. a Petition in Response to the Notice to File Corrected Application Papers having attached thereto:
 - Exhibit A a copy of the return postcard as evidence that 367 sheets of drawings were filed with the original divisional application; and
 - Exhibit B a copy of the Utility Patent Application Transmittal form as evidence that 367 sheets of drawings were filed with the original divisional application;
- one copy each of Figures 40A and 81A that were filed as part of the 367 sheets of drawings;
- 3. a revised abstract, not exceeding 250 words in accordance with MPEP 608.01(b), in addition to a clean copy of the revised abstract;

00303274

- 4. a copy of the "Notice to File Corrected Application Papers" (Form PTO-1533); and
- 5. a check for \$130.00 to cover the petition fee under 37 C.F.R. 1.117(h), which will be refunded if the Petition in Response to the Notice to File Drawings is granted.

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to our Deposit Account No. 20-0888. A copy of this transmittal letter is enclosed.

A return postcard is also enclosed. Please date stamp and mail the postcard in order to acknowledge receipt of this correspondence.

Respectfully submitted,

Edward L. Pencoske

Reg. No. 29,688

THORP, REED & ARMSTRONG, LLP

One Oxford Centre

301 Grant Street, 14th Floor

Pittsburgh, PA 15219-1425

(412) 394-7789

Dated: ____June, 2001

Attorneys for Applicants

ABSTRACT

A 256 Meg dynamic random access memory is comprised of a plurality of cells organized into individual arrays. [with the arrays being] which are reganized into 32 Meg array blocks, which are organized into 64 Meg quadrants. Sense amplifiers are positioned between adjacent rows in the individual arrays while; row decoders are positioned between adjacent columns in the individual arrays. In certain of the gap cells, multiplexers are provided to transfer signals from I/O lines to data lines. A datapath is provided which, in addition to the foregoing, includes array I/O blocks, responsive to the datalines from each quadrant to output data to a data read mux, data buffers, and data driver pads. The write data path includes a data in buffer and data write muxes for providing data to the array I/O blocks. A power bus is provided which minimizes routing of externally supplied voltages, completely rings each of the array blocks, and provides gridded power distribution within each of the array blocks. A plurality of voltage supplies provide the voltages needed in the array and in [the] peripheral circuits. The power supplies are organized to match their power output to the power demand and to maintain a desired ratio of power production capability and decoupling capacitance. A powerup sequence circuit is provided to control the powerup of the chip. Redundant rows and columns are provided as is the circuitry necessary to logically replace defective rows and columns with operational rows and columns. Circuitry is [also] provided on chip to support various types of test modes.